UNITED STATES PATENT AND TRADEMARK OFFICE

NC

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,595	06/18/2001	Quat T. Vu	42390P10889	3197

8791 7590 08/22/2003

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER
WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,595	VU ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *15-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Serial Number: 09/884595 Attorney's Docket #: 42P10889
Filing Date: 6/18/2001;

Applicant: Vu et al.

Examiner: Alexander Williams

The disclosure is objected to because of the following informalities: The related application information should be updated.

Appropriate correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second interconnection layer comprises **at least one dielectric layer abutting at least one of said microelectronic device back surface**, said microelectronic substrate core second surface, and said encapsulant material second surface, and at least one conductive trace disposed on said at least one dielectric layer in claim 8 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claims 8 to 12 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 8, it is unclear and confusing to what is meant by "wherein said second interconnection layer comprises **at least one dielectric layer abutting at least one of said microelectronic device back surface**, said microelectronic substrate core second surface, and said encapsulant material second surface, and at least one conductive trace disposed on said at least one dielectric layer."

In claim 10, line 13, "said microelectronic die" needs to be identified to which die back should be defined.

Any of claims 8 to 12 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 3, 5 to 9, 13 and 14, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Miles et al. (U.S. Patent # 5,696,666).

I. Miles et al. (figures 1 to 4) specifically figure 4 show a microelectronic substrate **40**, comprising: a first microelectronic substrate core **14** having a first surface and an opposing second surface, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface; at least one first microelectronic device **12** disposed within said at least one opening, said at least one first microelectronic device having an active surface and a back surface, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface; an encapsulation material **24** adhering said first microelectronic substrate core to said at least one first microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface; and at least one conductive via **20** extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface.

2. The microelectronic substrate of claim 1, Miles et al. further including a first interconnection layer disposed proximate said first microelectronic substrate core first surface and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said first microelectronic substrate core second surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer.

3. The microelectronic substrate of claim 2, Miles et al. further including at least one microelectronic device attached to at least one of said first interconnection layer and said second interconnection layers.

5. The microelectronic substrate of claim 2, Miles et al. showing wherein said first interconnection layer comprises at least one dielectric layer abutting at least one of said first microelectronic device active surface, said first microelectronic substrate core first surface, and said encapsulation material first surface, and at least one conductive trace disposed on said at least one dielectric layer.

2. The microelectronic substrate of claim 1, Miles et al. further including a first interconnection layer disposed proximate said first microelectronic substrate core first surface and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said first microelectronic substrate core second surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer.

3. The microelectronic substrate of claim 2, Miles et al. further including at least one microelectronic device attached to at least one of said first interconnection layer and said second interconnection layers.

5. The microelectronic substrate of claim 2, Miles et al. showing wherein said first interconnection layer comprises at least one dielectric layer abutting at least one of said first microelectronic device active surface, said first microelectronic substrate core first surface, and said encapsulation material first surface, and at least one conductive trace disposed on said at least one dielectric layer.

6. The microelectronic substrate of claim 5, Miles et al. showing at least one conductive trace extends through said at least one dielectric layer to contact at least one electrical contact on said first microelectronic device active surface.

7. The microelectronic substrate of claim 5, Miles et al. showing wherein said at least one conductive trace extends through said at least one dielectric layer to contact said at least one conductive via.

8. The microelectronic substrate of claim 2, Miles et al. showing wherein said second interconnection layer comprises at least one dielectric layer abutting at least one of said microelectronic device back surface, said microelectronic substrate core second surface, and said encapsulant material second surface, and at least one conductive trace disposed on said at least one dielectric layer.

9. The microelectronic substrate of claim 8, Miles et al. showing wherein said at least one conductive trace extends through said at least one dielectric layer to contact said at least one conductive via.

13. Miles et al. (figures 1 to 4) specifically figure 4 show a microelectronic substrate **14**, comprising: at least one first microelectronic device **12** having an active surface and a back surface; an encapsulation material **42** forming a first surface adjacent said microelectronic die active surface and a second surface adjacent said microelectronic

die back surface; and at least one conductive via **20** extending from said encapsulation material first surface to said encapsulation material second surface.
14. The microelectronic substrate of claim 13, Miles et al. further including a first interconnection layer **18** disposed proximate said encapsulation material first surface and said first microelectronic device active surface and further including a second interconnection layer **18** disposed proximate said encapsulation material second surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer.

Claims 1 to 9, 13 and 14, **insofar as claims 8 and 9 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Towle et al. (U.S. Patent Application Publication # 2002/0137263 A1) in view of Eichelberger (U.S. Patent # 5,841,193).
1. Towle et al. (figures 3 to 21) specifically figure 21 show a microelectronic substrate **170**, comprising: a first microelectronic substrate core **102** having a first surface **148** and an opposing second surface **118**, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface; at least one first microelectronic device **114** disposed within said at least one opening, said at least one first microelectronic device having an active surface **116** and a back surface **118**, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface; an encapsulation material **144** adhering said first microelectronic substrate core to said at least one first microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface; but fail to explicitly show at least one conductive via extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface.
13. Towle et al. (figures 3 to 21) specifically figure 21 show a microelectronic substrate **102**, comprising: at least one first microelectronic device **102** having an active surface and a back surface; an encapsulation material **144** forming a first surface adjacent said microelectronic die active surface and a second surface adjacent said microelectronic

die back surface; but fail to explicitly show at least one conductive via extending from said encapsulation material first surface to said encapsulation material second surface.

Eichelberger is cited for showing single chip modules. Specifically, Eichelberger (figures 4 to 10) specifically figure 6 discloses a microelectronic substrate **200**, comprising: a first microelectronic substrate core **104** having a first surface **103'** and an opposing second surface **105'**, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface; at least one first microelectronic device **102** disposed within said at least one opening, said at least one first microelectronic device having an active surface and a back surface, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface; and explicitly show at least one conductive via **202** extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface for the purpose of providing an electronic packaging and interconnect means where both defective chips and defective interconnect can be replaced in the finished modules.

2. The microelectronic substrate of claim 1, the combination with Eichelberger further including a first interconnection layer disposed proximate said first microelectronic substrate core first surface and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said first microelectronic substrate core second surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer.

3. The microelectronic substrate of claim 2, the combination with Eichelberger further including at least one microelectronic device attached to at least one of said first interconnection layer and said second interconnection layers.

4. The microelectronic substrate of claim 2, the combination with Eichelberger further including at least one heat dissipation device thermally attached to said at least one microelectronic device back surface.

5. The microelectronic substrate of claim 2, the combination with Eichelberger showing wherein said first interconnection layer comprises at least one dielectric layer abutting at least one of said first microelectronic device active surface, said first microelectronic substrate core first surface, and said encapsulation material first surface, and at least one conductive trace disposed on said at least one dielectric layer.

6. The microelectronic substrate of claim 5, the combination with Eichelberger showing wherein said at least one conductive trace extends through said at least one dielectric layer to contact at least one electrical contact on said first microelectronic device active surface.
7. The microelectronic substrate of claim 5, the combination with Eichelberger showing wherein said at least one conductive trace extends through said at least one dielectric layer to contact said at least one conductive via.
8. The microelectronic substrate of claim 2, the combination with Eichelberger showing wherein said second interconnection layer comprises at least one dielectric layer abutting at least one of said microelectronic device back surface, said microelectronic substrate core second surface, and said encapsulant material second surface, and at least one conductive trace disposed on said at least one dielectric layer.
9. The microelectronic substrate of claim 8, the combination with Eichelberger showing wherein said at least one conductive trace extends through said at least one dielectric layer to contact said at least one conductive via.
14. The microelectronic substrate of claim 13, the combination with Eichelberger further including a first interconnection layer disposed proximate said encapsulation material first surface and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said encapsulation material second surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Eichelberger's conductive via in the substrate to modify Towle et al.'s substrate for the purpose of providing an electronic packaging and interconnect means where both defective chips and defective interconnect can be replaced in the finished modules.

The following references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/782,774,680,700-703, 723,685,686,690-693,696,698,684,796 174/52.1,52.2,52.3,52.4	8/13/03
Other Documentation: foreign patents and literature in 257/782,774,680,700-703, 723,685,686,690-693,696,698,684,796 174/52.1,52.2,52.3,52.4	8/13/03
Electronic data base(s): U.S. Patents EAST	8/13/03

Papers related to this application may be submitted to Technology Center 2800 by facsimile transmission. Papers should be faxed to Technology Center 2800 via the Technology Center 2800 Fax center located in Crystal Plaza 4-5B15. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Technology Center 2800 Fax Center number is (703) 308-7722 or 24. Only Papers related to Technology Center 2800 APPLICATIONS SHOULD BE FAXED to the GROUP 2800 FAX CENTER.

Any inquiry concerning this communication or any earlier communication from the examiner should be directed to ***Examiner Alexander Williams*** whose telephone number is **(703) 308-4863**.

Any inquiry of a general nature or relating to the status of this application should be directed to the ***Technology Center 2800 receptionist*** whose telephone number is **(703) 308-0956**.

8/14/03

Primary Patent Examiner
Alexander O. Williams